Amendments to the Claims:

1. (currently amended) A circuit for measuring distances, comprising at least two inputs, at least one measuring coil, and at least one signal source for generating at least two input signals, wherein the at least two inputs are activatable by means of the input signals, wherein the input signals are applied to the inputs of the measuring coil, and wherein the input signals are applied to at least one SC network and used for generating a measuring ~~signal and/or an~~ output signal that is dependent on a temperature influence, said at least one SC network comprising

a) a first SC unit connected to one of the input signals,

b) a second SC unit connected to the other of the input signals, and

c) a third SC unit connected to the outputs of the first and second SC units so as to combine the outputs of the first and second SC units.

2. (currently amended) The circuit of claim 1, wherein the at least two input signals are essentially unipolar or ~~and/or~~ in phase opposition.

3. (currently amended) The circuit of claim 1, wherein the input signals are filtered proportionately by means of at least one filter or ~~and/or~~ by means of a high-pass.

4. (original) The circuit of claim 1, wherein the at least one SC network includes at least one SC amplifier.

5. (currently amended) The circuit of claim 4, wherein a first SC amplifier is configured as a positive delayed SC amplifier or ~~and/or~~ multiplies the two inputs with respectively one factor.

6. (currently amended) The circuit of claim 4, wherein a second SC amplifier is configured as a positive delayed SC amplifier, or ~~and/or~~ delays one of the input signals by one half period of a clock frequency.

7. (original) The circuit of claim 1, wherein the SC network includes at least one SC integrator.

8. (currently amended) The circuit of claim 7, wherein the SC integrator is configured as a negative undelayed SC integrator, or ~~and/or~~ includes an amplification of 1, or ~~and/or~~ is a lossy SC integrator.

9. (original) The circuit of claim 1, wherein the at least one SC network includes a first SC amplifier, a second SC amplifier, and an SC integrator having an output which is applied to a second input of the first SC amplifier.

10. (original) The circuit of claim 9, wherein the outputs of the first SC amplifier and the second SC amplifier are added by means of an SC adder.

11. (currently amended) The circuit of claim 10, wherein the output of the first amplifier is applied to the inputs of the SC integrator or ~~and/or~~ the SC adder.

12. (original) The circuit of claim 11, wherein the output of the second SC amplifier is applied to a second input of the SC adder.

13. (original) The circuit of claim 10, wherein the first and the second SC amplifier, and the SC adder are configured as negative undelayed circuits.

14. (original) The circuit of claim 13, wherein the SC integrator is configured as a positive delay circuit.

15. (original) The circuit of claim 10, wherein the SC adder produces an output signal which is inverted.

16. (original) The circuit of claim 1, wherein the SC network includes at least one SC amplifier, and at least one SC integrator, and at least one SC difference amplifier.

17. (original) The circuit of claim 16, wherein the circuit is configured such that at least one of the input signals is multiplied by a factor and stored in the SC integrator.

18. (original) The circuit of claim 17, wherein the circuit is configured such that the factor is erased by a capacitance of the SC integrator during each clock period.

19. (original) The circuit of claim 16, wherein the at least one SC amplifier is configured as a positive delayed SC amplifier which delays at least one of the input signals unamplified by a half period of a clock frequency.

20. (currently amended) The circuit of claim 16, wherein the outputs of the SC amplifier and the SC integrator are subtracted by means of the SC difference amplifier or ~~and/or~~ be delayed by a half period of a clock frequency.

21. (original) The circuit of claim 16, wherein the output of the SC amplifier is applied to a second input of the SC integrator.

22. (original) The circuit of claim 1, wherein the at least one SC network generates an output signal which has a delay of one clock period.

23. (currently amended) A method for measuring distances, utilizing a measuring circuit which comprises at least two inputs, at least one measuring coil, and at least one signal source, comprising the steps of

generating at least two input signals by means of a signal source which are applied to the inputs and applied to inputs of the measuring coil, and including applying the input signals to at least one SC network which is configured for generating a measuring ~~signal and/or an~~ output signal that is dependent on temperature,

said at least one SC network comprising

a) a first SC unit connected to one of the input signals,

b) a second SC unit connected to the other of the input signals, and

c) a third SC unit connected to the outputs of the first and second SC units so as to combine the outputs of the first and second SC units.

24. (new) The circuit of Claim 1, wherein the first and second SC units process the respective input signals differently.

25. (new) The circuit of Claim 24, wherein the first and second SC units are configured for adding, or subtracting, or amplifying, or integrating the respective inputs signals.

26. (new) The circuit of Claim 24, wherein the third SC unit comprises a SC adder or a SC difference amplifier.